FORM PTO-1390 (Modified) (REV 10-95) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY'S DOCKET NUMBER	U.S. APPLICATION NO. (IF KNOWN, SEE 37 CFR)
199649US2PCT	09/701391

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/FR99/01287	02 June 1999	03 June 1998

TITLE OF INVENTION
A RECEIVER FOR A CDMA SYSTEM

APPLICANT(S) FOR DO/EO/US
Laurent OUVRY, et al.

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☒ This is an express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39(1).
4. ☒ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.
5. ☒ A copy of the International Application as filed (35 U.S.C. 371 (c) (2))
   a. ☐ is transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☒ has been transmitted by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☒ A translation of the International Application into English (35 U.S.C. 371(c)(2)).
7. ☒ A copy of the International Search Report (PCT/ISA/210).
8. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371 (c)(3))
   a. ☐ are transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ have been transmitted by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☒ have not been made and will not be made.
9. ☐ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
10. ☒ An oath or declaration of the inventor(s) (35 U.S.C. 371 (c)(4)).
11. ☐ A copy of the International Preliminary Examination Report (PCT/IPEA/409).
12. ☐ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371 (c)(5)).

Items 13 to 18 below concern document(s) or information included:

13. ☐ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
14. ☐ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
15. ☐ A **FIRST** preliminary amendment.
    A **SECOND** or **SUBSEQUENT** preliminary amendment.
16. ☐ A substitute specification.
17. ☐ A change of power of attorney and/or address letter.
18. ☐ Certificate of Mailing by Express Mail
19. ☒ Other items or information:

Request for Consideration of Documents Cited in International Search Report
Notice of Priority
PCT/IB/304
PCT/IB/308
Drawings (5 Sheets)

525 Rec'd PCT/PTO 04 DEC 2000

U.S. APP: 09/701391	INTERNATIONAL APPLICATION NO. PCT/FR99/01287	ATTORNEY'S DOCKET NUMBER 199649US2PCT

20. The following fees are submitted:.		CALCULATIONS PTO USE ONLY
BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) - (5)) :		
☒ Search Report has been prepared by the EPO or JPO	$860.00	
☐ International preliminary examination fee paid to USPTO (37 CFR 1.482)	$690.00	
☐ No international preliminary examination fee paid to USPTO (37 CFR 1.482) but international search fee paid to USPTO (37 CFR 1.445(a)(2))	$710.00	
☐ Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2) paid to USPTO	$1000.00	
☐ International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(2)-(4)	$100.00	

ENTER APPROPRIATE BASIC FEE AMOUNT =				$860.00	
Surcharge of **$130.00** for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492 (e)).				**$0.00**	
CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE		
Total claims	1 - 20 =	0	x $18.00	$0.00	
Independent claims	0 - 3 =	0	x $80.00	$0.00	
Multiple Dependent Claims (check if applicable).			☐	**$0.00**	
TOTAL OF ABOVE CALCULATIONS =				$860.00	
Reduction of 1/2 for filing by small entity, if applicable. Verified Small Entity Statement must also be filed (Note 37 CFR 1.9, 1.27, 1.28) (check if applicable).			☐	**$0.00**	
SUBTOTAL =				$860.00	
Processing fee of **$130.00** for furnishing the English translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492 (f)).			+	**$0.00**	
TOTAL NATIONAL FEE =				$860.00	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31) (check if applicable).			☐	**$0.00**	
TOTAL FEES ENCLOSED =				$860.00	
				Amount to be: refunded	$
				charged	$

☒ A check in the amount of $860.00 to cover the above fees is enclosed.

☐ Please charge my Deposit Account No. in the amount of to cover the above fees.
A duplicate copy of this sheet is enclosed.

☒ The Commissioner is hereby authorized to charge any fees which may be required, or credit any overpayment to Deposit Account No. 15-0030 A duplicate copy of this sheet is enclosed.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

22850

Surinder Sachar
Registration No. 34,423

Surinder Sachar
SIGNATURE

Marvin J. Spivak
NAME

24,913
REGISTRATION NUMBER

Dec. 4 2000
DATE

A RECEIVER FOR A CDMA SYSTEM

Technical Field

The object of the present invention is a receiver for a CDMA system, i.e. for code division multiple access systems, a technology known in English by the abbreviation CDMA. More generally, this technology falls within the framework of digital transmission with direct sequence spread spectrum (abbreviated to DSSS).

The invention finds applications in radiocommunications systems with mobiles, in wireless local area networks (WLAN), in wireless local loops (WLL), in cable television, etc.

Prior Art

It is assumed that the requirement is to transmit information constituted by a symbol stream of duration Ts, each symbol being able to be, for example, a bit equal to 0 or 1.

The direct sequence spread spectrum consists in modulating each symbol of the digital signal in a pseudorandom binary sequence. Such a sequence is composed of N pulses or "chips" the duration Tc of which is equal to Ts/N. The modulated signal has a spectrum which spreads over a range N times wider than that of the original signal. At reception, demodulation consists in correlating the signal with the sequence used at emission, which allows the information linked to the start symbol to be relocated.

The advantages of this technology are manifold:

- discretion, since the power spectral density of the signal is reduced by a factor N;
- immunity in respect of wanted or parasitic narrow band emissions, since the correlation operation carried out at receiver level leads to the spread spectrum of these emissions;
- difficult interception since demodulation requires knowledge of the sequence used at emission;
- resistance to multiple channels which, under certain conditions, cause selective fading in frequency and therefore only partially affect the signal emitted;
- possible multiple access by allocation of different sequences to different users.

Turning this last advantage to good account, CDMA technology consists of the simultaneous emission, in a same band, of several spread signals using different pseudorandom spread sequences. The sequences are chosen so that the intercorrelations remain small.

If the different emitters do not have a common time reference, the system is said to be asynchronous since the beginnings of the symbols particular to each user reach the receiver at different moments. This is shown in the appended Figure 1 where the lines in the left hand part show the time for three different users 1, 2, and 3 and the arrows pointing upwards show the emission start moments (the "tops") of the symbols. The central part shows symbolically the paths towards a same receiver. The right hand part shows the time position of the beginnings of the symbols received for each of the users, i.e.,

lastly, the dephases of the symbols of the different users relative to each other.

It can be arranged for the beginnings of the symbols received 1, 2 and 3 to coincide (modulo the period Ts of a symbol). The system is then said to be "synchronous". It is shown in Figure 2 with the same conventions.

In an asynchronous CDMA system, the sequences have any relative phases at reception. A good separation of the signals presupposes therefore that the intercorrelations between sequences are small, whatever the relative phases between sequences. On the other hand, in synchronous CDMA, the sequences arriving with nil relative phases, the number of intercorrelations having to be close to zero is much smaller. This particularity gives the synchronous system a very clear advantage over the asynchronous variant in terms of the number of sequences (therefore of users) being able to coexist without mutual totally unacceptable disturbance.

These questions can be made rather clearer by giving an expression of the signal emitted and of the signal received. It will be hypothetically assumed that the different sequences linked to each symbol are synchronous. This implies that the number N, length of sequences counted as a number of chips, takes the same value whatever the sequence (or the emission) concerned.

Given these hypotheses, the emitted signal may be expressed, in base-band, by an emitter of rank k by the expression:

$$S_k(t) = A_k \sum_{i=0}^{+\infty} a_k(i) \sum_{j=0}^{N-1} c_k(j)\, p(t - jT_c - iNT_c + \tau_{0k})$$

with:

- A_k : amplitude of the signal emitted by the user of rank k,
- $a_k(i)$: symbols of rank i emitted by the user k,
- $c_k(j)$: chip of rank j of the sequence k,
- T_c: chip time,
- p(.) : chip form; this is most often a rectangular pulse different from zero between 0 and Tc,
- τ_{0k}: signal k delay (or advance).

It is assumed, so as to simplify the model that the channels are not selective in frequency.

The pulse response of a channel for the user of rank k is:

$$h_k(t) = g_k \delta(t - \tau_k)$$

with:

- g_k: complex gain corresponding to the channel of rank k,
- τ_k: delay introduced by the channel k,
- δ: Dirac pulse.

The signal received may be written in the form:

$$r(t) = \sum_{k=0}^{k-1} S_k(t) * h_k(t)$$

where the sign * indicates a convolution product This expression may further be written:

$$r(t) = \sum_{k=0}^{k-1} g_k A_k \sum_{i=0}^{+\infty} a_k(i) \sum_{j=0}^{N-1} c_k(j)\, p(t - jT_c - iNT_c + \tau_{0k} - \tau_k)$$

If the system is synchronous, then $\tau_{0k}-\tau_k=\tau$ whatever k may be where τ is anything. Thus, in emitters, the τ_{0k} must be adjusted so that this relation is verified.

In the event of there being only one emitting source, this condition would obviously be fulfilled.

The appended Figure 3 shows the principle of a spread spectrum signal receiver. The receiver shown includes a first circuit 10, which can be an adapted filter or a sliding correlator, a recovery circuit 12 of a symbol clock signal, a signal which allows synchronisation of the receiver means, possibly a processing circuit 14 able to effect different additional processes, such as for example a delayed multiplication, a channel estimation etc., and lastly a circuit 16 able to make a decision on the value of the symbol transmitted.

If there are several users, therefore several distinct sequences, the receiver includes as many channels as sequences, as shown in Figure 4, with channels V_1, V_2, ..., V_k where K is the number of users (or sequences). Each channel restores the symbols d_1, d_2, ..., d_k, particular to its sequence, therefore to the user.

Components are commercially available today to make such receivers. As an example the following may be quoted:

- the component HFA 3860 of the Harris company, which uses a bank of 8 sliding correlators (called serial correlators) arranged in parallel (as shown in Figure 4); symbol clock recovery is effected by means of a transmission preamble;
- the component SC2001 of the Sirius Communications company, which incorporates a bank of sliding

correlators allowing a signal with two synchronous users to be processed.

The first circuit of each channel, whether it is a sliding correlator or an adapted filter, plays an important role which may be clarified by means of Figures 5 and 6.

A sliding correlator (Figure 5) includes diagrammatically a pseudorandom sequence generator 20 and a multiplier 22 receiving the input signal r(t) and the sequence delivered by the generator 20, an adder 24, a circuit 26 linked to the output of the adder 24 and relooped onto it and making a delay. The sliding correlator output is connected to a sub-sampler 28. The circuits 20, 26, 28 are controlled by a symbol clock signal Hs.

As for the adapted filter (Figure 6), this is in general a digital filter 30 the coefficients of which are adapted to the sequence used. This filter receives the input signal r(t) and delivers a filtered signal again applied to a sub-sampler 28. The latter is controlled by the symbol clock signal Hs, which fixes the symbol rate.

Seen from the output of the sub-sampler 28, these two architectures are equivalent. On the other hand, seen from the input of the sub-sampler 28, they are different since they do not deliver the same signal, as Figures 7, 8 and 9 show.

Figure 7, first of all, shows the output Sf of the adapted digital filter in Figure 6, in accordance with the rank n of the samples; Figure 8 the output Sc of the sliding correlator in Figure 5 when the emitted sequence local reply is aligned with the emitted sequence; and

Figure 9 the ouput Sc of this same sliding correlator when the sequence local reply is not aligned with the emitted sequence. The correlator peak carrying the information on the symbol is marked P in Figures 7 and 8.

It is clear, from these Figures, that the sliding correlator requires information linked to symbol timing, a signal called a "symbol clock" and denoted Hs, so that the sequence local reply is aligned with the sequence modulating the symbols received, otherwise demodulating the symbols is impossible (the case in Figure 9). The adapted filter does not require this information. Thus, what differentiates in the first instance a structure with a sliding correlator and a structure with an adapted filter, is that the first requires external synchronisation information.

An adapted filter enables symbol clock recovery, for example by recursive detection of the correlation peak on a window of N points (Figure 7). Symbol clock recovery is also possible by means of a sliding correlator, but in a more complex way; it is necessary to modify step by step the sequence local reply phase until the sliding correlator output corresponds to a power maximum, therefore to a correlation peak (the case in Figure 8).

If these two structures allow the symbol clock to be relocated, they do not do so with the same speed: the symbol clock recovery operation lasts at the most N symbol periods, i.e. NTs with a sliding correlator, whereas it requires only a single symbol period Ts with an adapted filter.

The advantage of the adapted filter is therefore obvious in terms of the rapidity of symbol clock signal

acquisition. Its disadvantage is its operational complexity, since its installation in the form of a digital filter with finite pulse response (working at the chip rate) requires N multiplications and N additions for each sample. Its structural complexity goes hand in hand with its operational complexity.

The sliding correlator only effects one multiplication and one addition for each new sample. If it is relatively ill adapted to clock recovery, it is on the other hand very advantageous in terms of operational complexity.

Thus, whether recourse is made to adapted filters or to sliding correlators certain disadvantages cannot be avoided. The purpose of the present invention is precisely to overcome these.

Disclosure of the invention

The invention proposes to combine the advantages of each of these structures (adapted filter and sliding correlator) by using, in a multiple channel receiver, an adapted filter in at least one channel, this in order to restore rapidly and efficiently the symbol clock, and by using sliding correlators in the other channels so as to benefit from their low level complexity, these correlators being controlled by the symbol clock signal produced by the adapted filter.

The receiver of the invention is thus a hybrid, in the sense that it includes at least one channel using an adapted filter and other channels using sliding correlators. The complexity of the receiver is reduced by the use of correlators, without the efficiency of the

symbol clock signal restoration suffering as a result since the latter is provided by an adapted digital filter.

It may be noted that in some mobile telephone installations both an adapted filter and sliding correlators can be found, the adapted filter delivering a synchronisation signal. But, in these installations, the filter is adapted to a very particular sequence called a pilot and not to the sequences used to carry information. This adapted filter only operates therefore at the moment of pilot symbol reception. The sliding correlations then process the sequences carrying the information, whereas the adapted filter is inoperative. Synchronisation is therefore obtained prior to demodulation.

In the present invention, the adapted filter processes symbols carrying the information and permanently maintains the clock signal necessary to sliding correlators.

When the synchronism between the sequences is not perfect, it is possible to use several channels of the type with adapted filter, (instead of just one) so as to produce several symbol clock signals slightly offset relative to each other.

In an exact way, the object of the invention is a receiver for a CDMA system, intended to receive signals corresponding to streams of spread spectrum information symbols in pseudorandom binary sequences, this receiver including K processing channels and being characterised in that at least one of these channels includes a filter adapted to one of the pseudorandom sequences having been used for information symbols spectrum spreading and a

symbol timing clock signal recovery circuit, the other channels each including a sliding correlator working with one of the other sequences having been used for information symbols spectrum spreading, each sliding correlator being controlled by a symbol clock signal, which is the clock signal produced by the channel using the adapted filter.

Brief Description of the drawings

- Figure 1, already described, shows the symbol beginning times for three users in an asynchronous CDMA system;
- Figure 2, already described, shows the symbol beginning times for three users in a synchronous CDMA system;
- Figure 3, already described, shows a known receiver architecture;
- Figure 4, already described, shows a multi-channel architecture in parallel;
- Figure 5, already described, shows a sliding correlator structure;
- Figure 6, already described, shows an adapted filter structure;
- Figure 7, already described, shows an adapted filter output;
- Figure 8, already described, shows a sliding correlator output when the sequence local reply is aligned with the sequence emitted;

- Figure 9, already described, shows a sliding correlator output when the sequence local reply is not aligned with the sequence emitted;
- Figure 10 shows an embodiment of a receiver according to the invention.

Description of a particular embodiment of the invention

Figure 10 shows a receiver according to the invention. This receiver includes K channels, V_1, V_2, ..., V_k of which one channel V_1 uses an adapted filter, whereas the K-1 other channels V_2, ..., V_k use a sliding correlator. More exactly, the channel V_1 includes a digital filter 25 the coefficients of which are adapted to the sequence Nº1 used at emission, a symbol clock Hs recovery circuit 12, an additional processing circuit 14_1, able to effect, for example, a delayed multiplication, a channel estimation, etc. and lastly a decision circuit 16_1 restoring the information d_1 particular to the user having used this first sequence.

The channel V_2 includes a sliding correlator 30_2, an additional processing circuit 14_2 and a decision circuit 16_2 delivering the restored information d_2. Likewise for the other channels, and in particular for the V_k, which includes a correlator 30_k, a processing circuit 14_k and a decision circuit 16_k restoring the information d_k. The correlators 30_2, ..., 30_k, require, as has been explained, a clock signal in order to be synchronised and this is constituted, in accordance with the invention, by the symbol clock Hs signal recovered in the first channel V_1.

This clock may also be applied to the circuits 14_1, 14_2, ..., 14_K and 16_1, 16_2, ..., 16_K.

Table 1 allows an architecture according to the invention to be compared with a conventional architecture using either sliding correlators, or adapted filters. The comparison is made in terms of operational complexity and symbol clock acquisition time (for K synchronous emitters and sequences of length N).

Table 1

	Receiver of the invention	Conventional receiver with adapted filters	Conventional receiver with sliding correlators
symbol clock acquisition time (by period Ts)	1	1	<N
Operational complexity (by number of multiplications per sampling period)	N+K-1	KN	K
Operational complexity (by number of additions per sampling period)	N+K-1	KN	K

By way of example, the case may be taken of K=64 synchronous users with sequences of N=128 chips:

- with a structure with 64 adapted filters, it is necessary to carry out 16,384 operations for each new sample, the acquisition being able to be achieved in 1 single symbol;
- with a structure with 64 sliding correlators, it is necessary to carry out 128 operations for each new sample, the acquisition being achieved in a maximum of 128 symbols;
- with a hybrid structure according to the invention, with 1 adapted filter and 127 sliding correlators, it is necessary to make 382

operations for each new sample, the acquisition being achieved in a single period.

From this example can be seen the excellent compromise obtained by the structure proposed by the invention. Moreover, it must be understood that a non hybrid structure with adapted filters would be excessively costly, if not even unrealisable on account of problems of size.

To sum up, the structure proposed by the invention makes it possible to:

- benefit from the synchronism between system users and from simultaneously acquiring the symbol clock of all users;
- profit from all the advantages of the structure with adapted filter;
- produce rapidly and reliably a symbol clock signal by using an adapted filter;
- pilot channels with sliding correlators with the symbol clock signal thus produced;
- benefit from the low level complexity of structures with sliding correlators;
- integrate, into a single circuit, the demodulation of a large number of emitters.

CLAIM

A receiver for a CDMA system, intended to receive signals corresponding to spread spectrum information symbol streams in pseudorandom binary sequences, this receiver including K processing channels (V_1, V_2, ..., V_k) being characterised in that at least one of these channels (V_1) includes a filter (20) adapted to one of the pseudorandom sequences having been used for information symbols spectrum spreading and a symbol clock signal (Hs) recovery circuit (12), the other channels (V_2, ..., V_k) each including a sliding correlator (30_2, ..., 30_k) working with one of the other sequences having been used for information symbols spectrum spreading, each sliding correlator being controlled by a symbol clock signal, which is the clock signal (Hs) produced by the channel (V_1) using the adapted filter (20).

DESCRIPTIVE ABSTRACT

A RECEIVER FOR A CDMA SYSTEM

The receiver includes at least one channel (V_1) with an adapted filter (20) and with a symbol clock signal (Hs) recovery circuit (12) and other channels (V_2, ..., V_k) with a sliding correlator (30_2, ..., 30_k) using the symbol clock signal (Hs) produced by the channel (V_1) with adapted filter.

Application for radiocommunications with mobiles.

Fig. 10

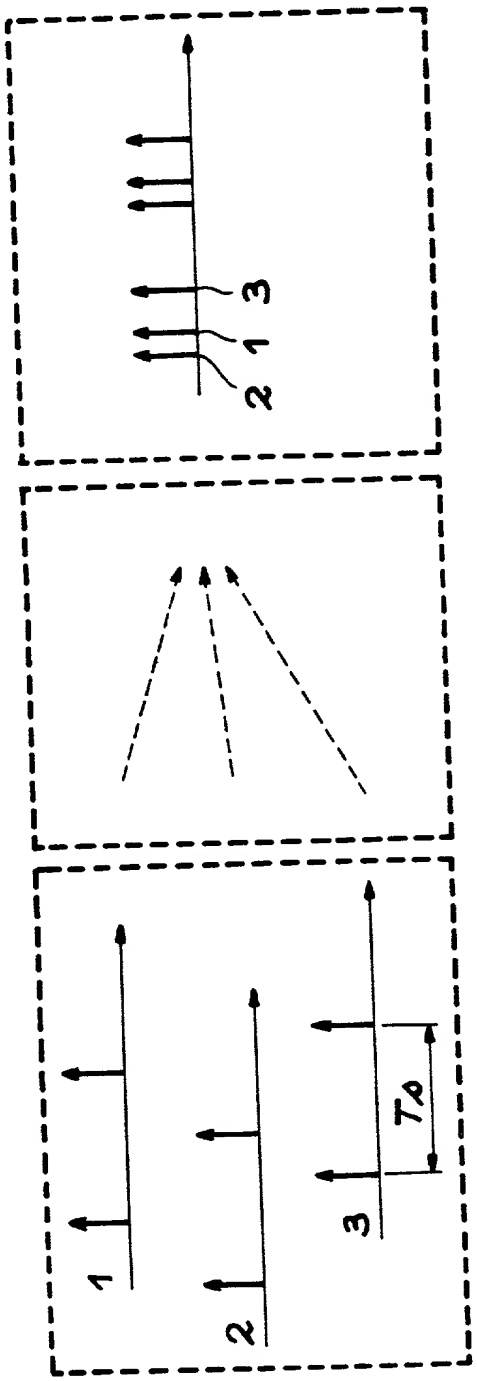


FIG. 1

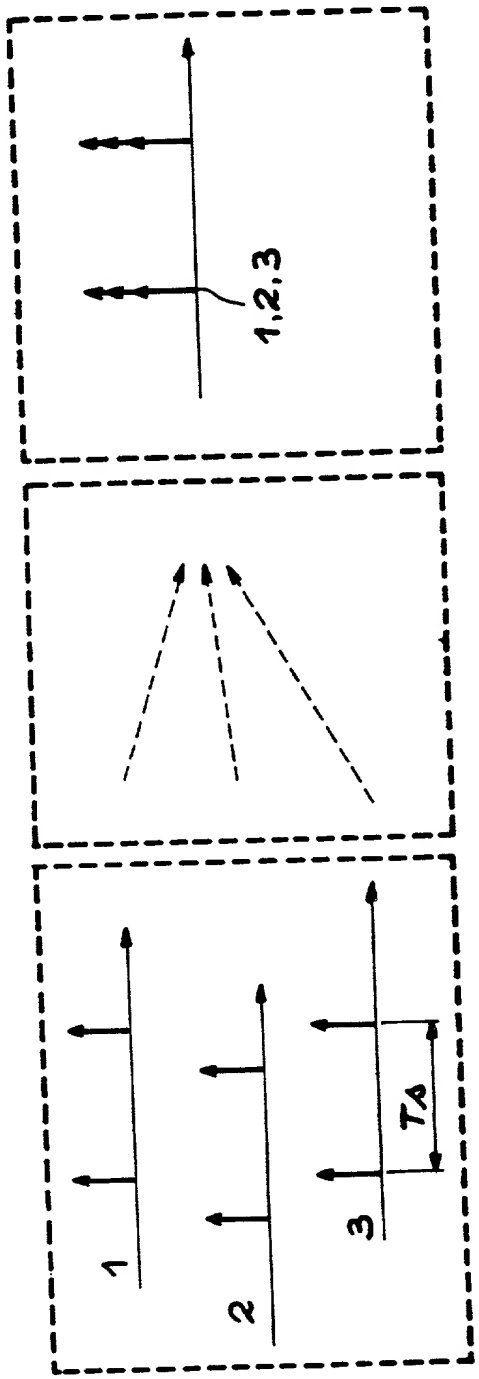


FIG. 2

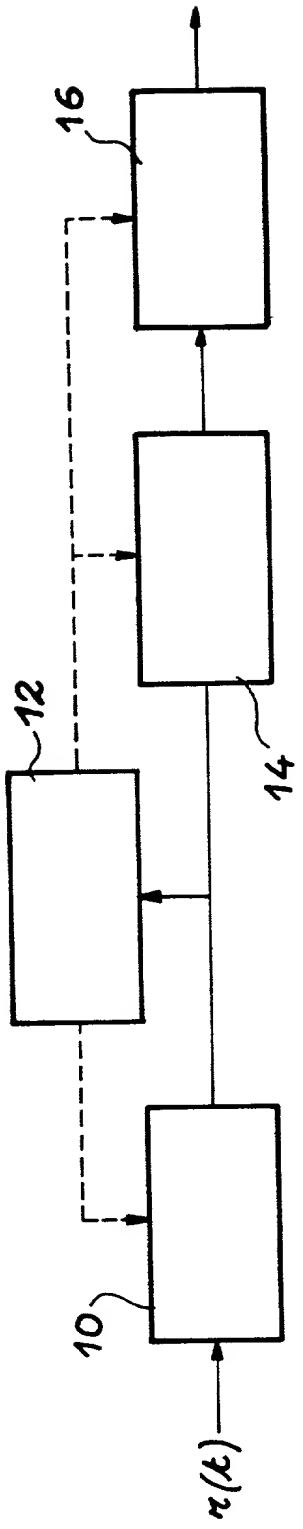


FIG. 3

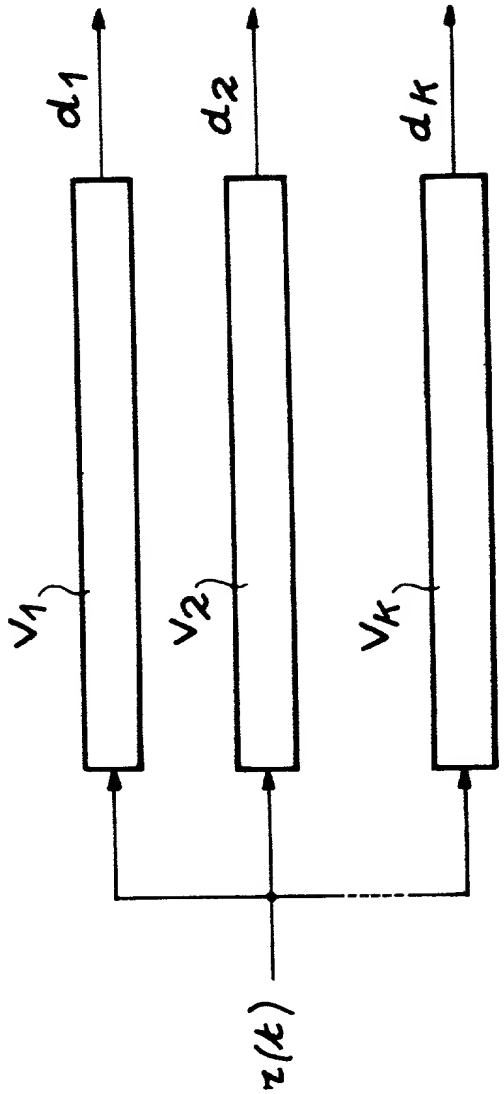


FIG. 4

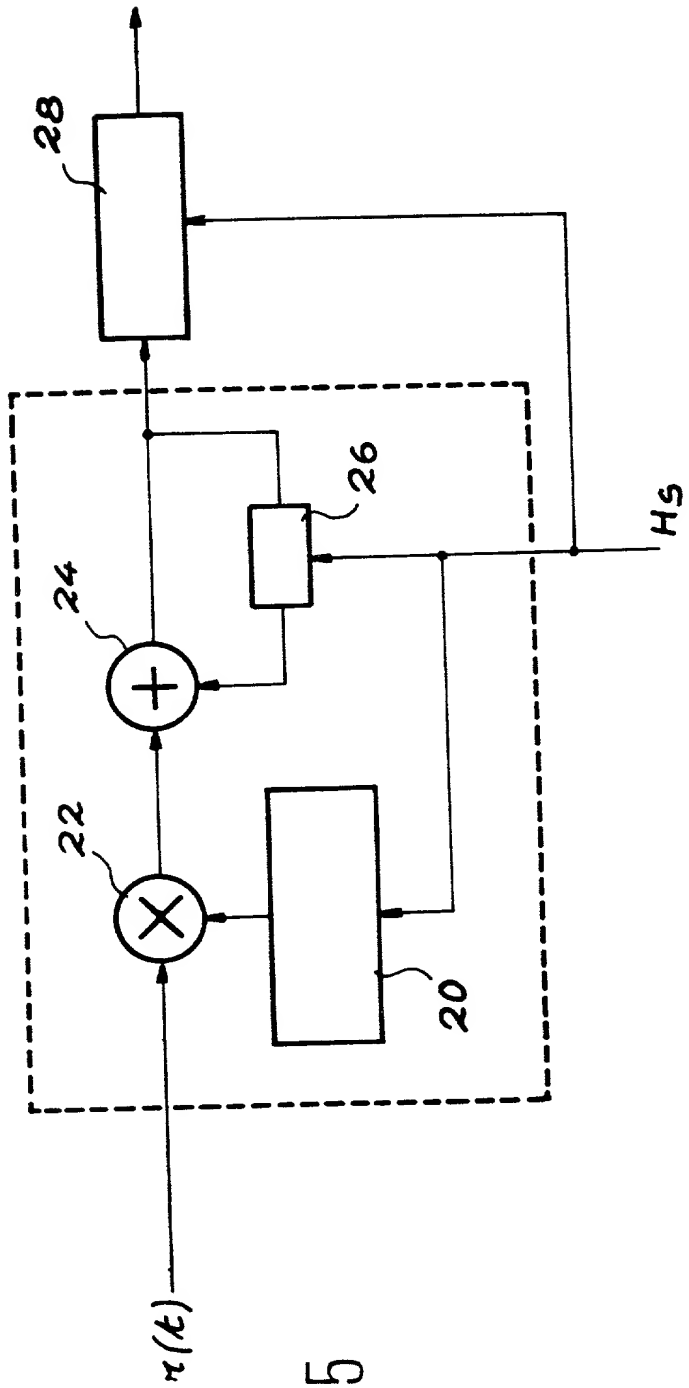


FIG. 5

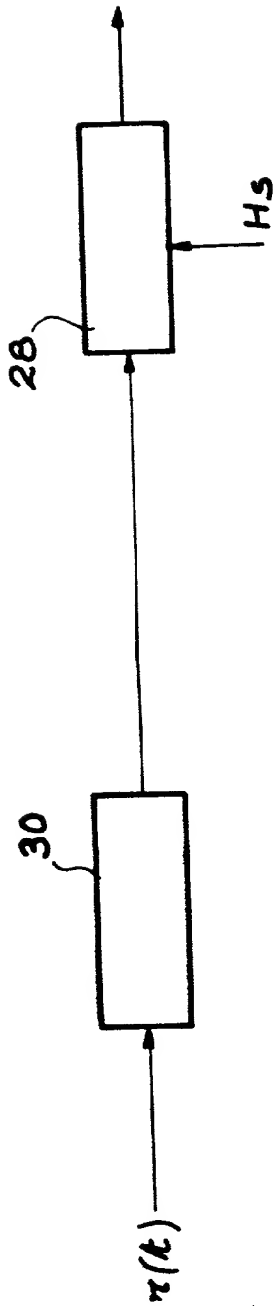


FIG. 6

FIG. 7

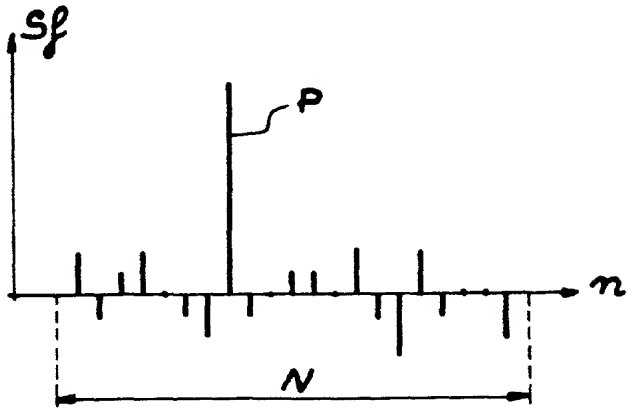


FIG. 8

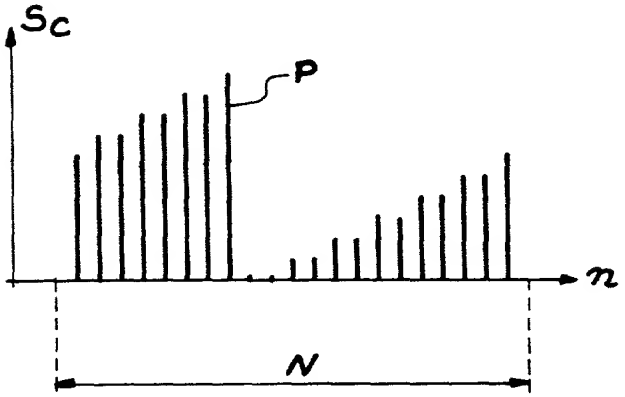
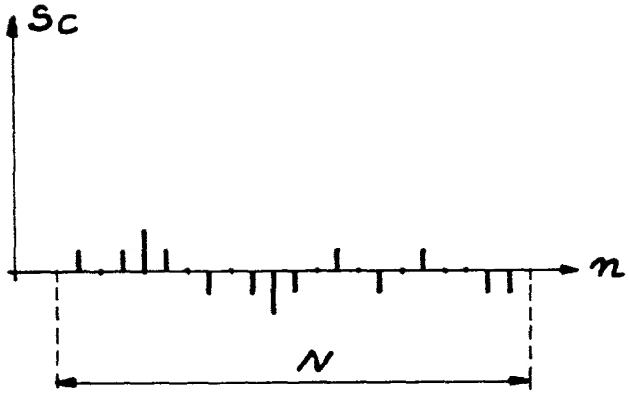


FIG. 9



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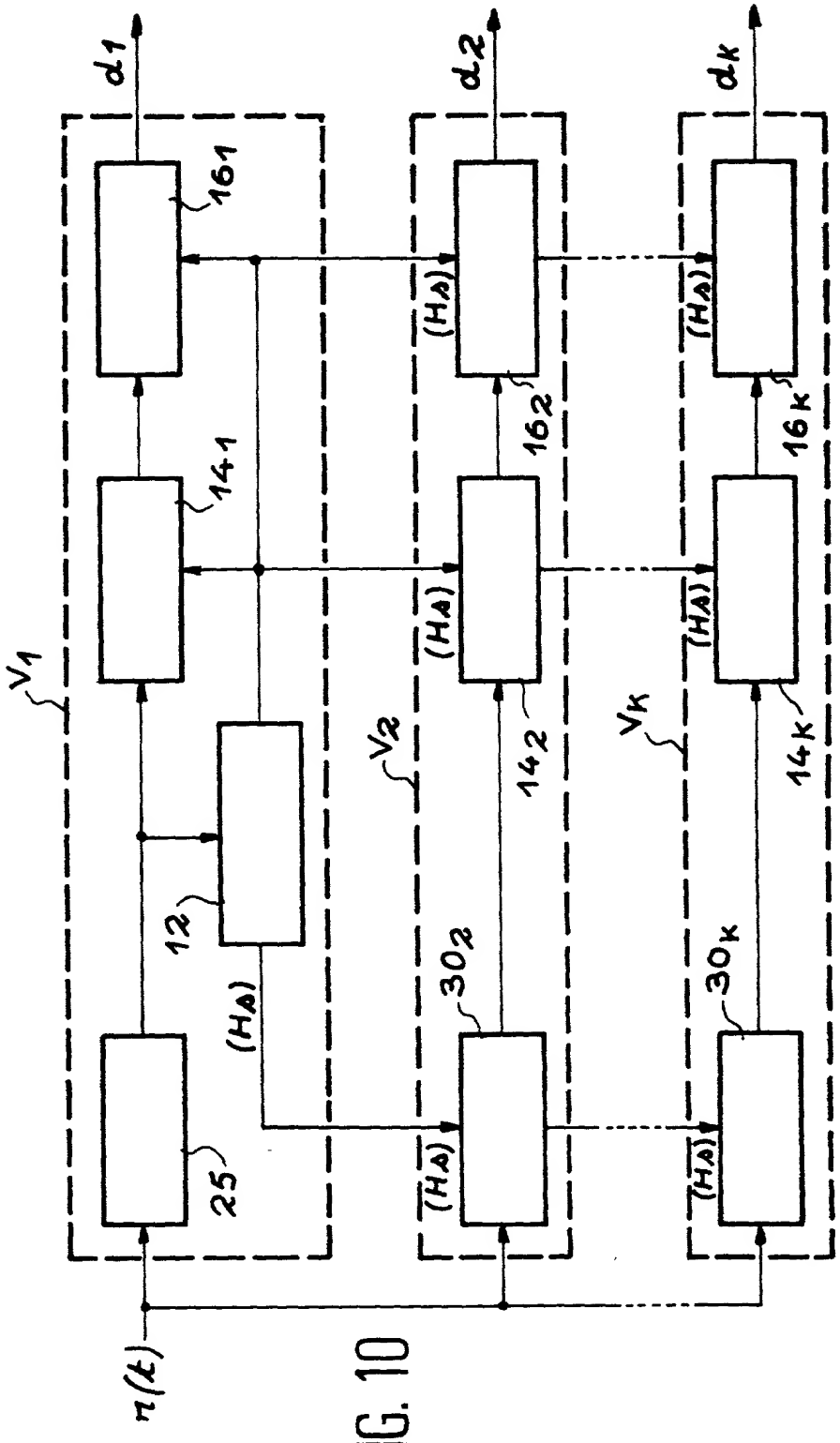

FIG. 10

B 13038.3 RS

Declaration, Power Of Attorney and Petition

WE (I) the undersigned inventor(s), hereby declare(s) that :

My residence, post office address and citizenship are as stated below next to my name,

We (I) believe that we are (I am) the original, first, and joint (sole) inventor(s) of the subject matter which is claimed and for which a patent is sought on the invention entitled

"A RECEIVER FOR A CDMA SYSTEM"

the specification of which

☐ is attached hereto.

☐ was filed on

as Application Serial No.

and amended on

☒ was filed as PCT international application

Number PCT/FR99/01287

on June 02, 1999

and was amended under PCT Article 19

on

We (I) hereby state that we (I) have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

We (I) acknowledge the duty to disclose information known to be material to the patentability of this application as defined in Section 1.56 of Title 37 Code of Federal Regulations.

We (I) hereby claim foreign priority benefits under 35 U.S.C. § 119 (a)-(d) or § 365 (b) of any foreign application(s) for patent or inventor's certificate, or § 365 (a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed. Prior Foreign Application (s)

Application No.	Country	Day/month/Year	Priority Claimed
98 06952	FRANCE	03 JUNE 1998	☒ YES ☐ NO
			☐ YES ☐ NO
			☐ YES ☐ NO
			☐ YES ☐ NO

We (I) hereby claim the benefit under Title 35, United States Code, § 119 (e) of any United States provisional application(s) listed below.

(Application Number) (Filing Date)

(Application Number) (Filing Date)

We (I) hereby claim the benefit under 35 U.S.C. §120 of any United States application(s), or § 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U.S.C. § 112, I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR § 1.56 which became available between the filing date of prior application and the national or PCT International filing date of this application.

Application Serial No.	Filing Date	Status (pending, patented, abandoned)

And we (I) hereby appoint : Norman F. Oblon, Registration Number 24,618; Marvin J. Spivak, Registration Number 24,913; C, Irvin McClelland, Registration Number 21,124; Gregory J. Maier, Registration Number 25,599; Arthur I. Neustadt, Registration Number 24,854; Richard D. Kelly, Registration Number 27,757; James D. Hamilton, Registration Number 28,421; Eckhard H. Kuesters, Registration Number 28,870; Robert T. Pous, Registration Number 29,099; Charles L. Gholz, Registration Number 26,395; William E. Beaumont, Registration Number 30,996; Jean-Paul Lavalleye, Registration Number 31,451; Stephen G. Baxter, Registration Number 32,884; Richard L. Treanor, Registration Number 36,379; Steven P. Weihrouch, Registration Number 32,829; John T. Goolkasian, Registration Number 26,142; Richard L. Chinn, Registration Number 34,305; Steven E. Lipman, Registration Number 30,011; Carl E. Schlier, Registration Number 34,426; James J. Kulbaski, Registration Number 34,648; Richard A. Neifeld, Registration Number 35,299; J. Derek Mason, Registration Number 35,270; Surinder Sachar, Registration Number 34,423; Christina M. Gadiano, Registration Number 37,628; Jeffrey B. McIntyre, Registration Number 36,867; William T. Enos, Registration Number 33,128; Michael E. McKabe Jr., Registration Number 37,182, Bradley D. Lytle, Registration Number 40,073 and Michael R. Casey Registration Number 40,294 ; our (my) attorneys, with full powers of substitution and revocation, to prosecute this application and to transact all business in the Patent Office connected therewith; and we (I) hereby request that all correspondence regarding this application be sent to the firm of OBLON, SPIVAK, McCLELLAND, MAIER & NEUSTADT, P.C., whose post Office Address is : Fourth Floor, 1755 Jefferson Davis Highway, Arlington, Virginia 22202.

We (I) declare that all statements made herein of our (my) own knowledge are true and that all statements made on information and belief are believed to be true ; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such wilful false statements may jeopardise the validity of the application or any patent issuing thereon.

OUVRY Laurent

NAME OF FIRST SOLE INVENTOR

Residence : 33 av Jeanne d'Arc
38100 Grenoble
FRANCE

Signature of Inventor

Citizen of : France

16 novembre 2000

Date

Post Office Address : The same as residence

2-00

LATTARD Didier

NAME OF SECOND INVENTOR

Signature of Inventor

16 novembre 2000

Date

Residence : Les Rithons

38680 RENCUREL FRX

FRANCE

Citizen of : France

Post Office Address : The same as residence

3-00

LEQUEPEYS Jean-René

NAME OF THIRD INVENTOR

Signature of Inventor

16 novembre 2000

Date

Residence : 4 rue de la Republique

38600 ~~France~~ Fontaine

FRANCE FRX

Citizen of : France

Post Office Address : The same as residence

NAME OF FOURTH INVENTOR

Signature of Inventor

Date

Residence :

Citizen of :

Post Office Address : The same as residence

NAME OF FIFTH INVENTOR

Signature of Inventor

Date

Residence :

Citizen of :

Post Office Address : The same as residence